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September 1999, Santa Clara, California (Proceedings  
Of Spie--the International Society For Optical  
Engineering, V. 3883.)**

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chip edge length at the 22 nm technology node. r Interconnect Technology Robust multi-level current-mode on- chip

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Multilevel interconnect technology III : 22-23 September SPIE--the International Society for Optical Engineering, 22-23 September 1999, Santa Clara, California".

**Patent us5055426 - method for forming a multilevel**

A method for forming lower levels of metal in multilevel interconnects involves initial formation of a poly-metal dielectric layer having grooves and contact holes,

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Society of Photo-Optical Instrumentation Engineers 1. 1999, Santa Clara, California ISBN Image and Signal Processing for Remote Sensing V: 22-24 September

**Conference papers and presentations | statistical**

Spatial Variation Decomposition via Sparse Regression, International Conference on IC Design and Technology (ICICDT), Austin, TX, May 2012. \*\*

**Thermal scaling analysis of multilevel cu/low-k**

Pradeep Teregowda): This paper presents a comprehensive thermal scaling analysis of multilevel the interconnect in Deep Nanometer Scale Technologies }

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Multilevel interconnect technology III : ( Santa Clara CA, 22-23 September 1999 ) Multilevel Society of Photo-Optical Instrumentation Engineers,

**Stochastic multilevel interconnect modeling and**

Interconnect Technology and Design for and P. Yang, Multilevel metal capacitance models for cad design Stochastic Multilevel Interconnect Modeling

**Patent us5372969 - low-rc multi-level interconnect**

A high-performance "low-RC" multi-level interconnect technology has been conceived for etc.), (ii) free-space interlevel dielectrics; (iii) 22 Sep 2006: 23

**Nonlinear optics lab publications - eth z**

California, SPIE, (The International Society for SPIE, (The International Society for Optical Engineering, III, Proceedings of the Third International

### **Brevetto us5451551 - multilevel metallization**

A maskless process for forming a protected metal feature in a planar insulating layer of a substrate is disclosed. A first barrier material is disposed in a recess in

### **Interconnect opportunities for gigascale**

New and radically different interconnect technologies will become and beyond the 22-nm technology in a multilevel interconnect network because

### **Geoffrey w. burr - ibm**

Santa Clara, California, Memory," 2010 IEEE International Interconnect Technology optical storage," Proceedings of the SPIE, Vol

### **Multilevel interconnect technology iii : 22-23**

A selection of 19 scientific papers addressing multilevel interconnect technology from a number of perspectives.

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### **Multilevel interconnect technology iii: 22- 23**

Multilevel Interconnect Technology III: 22-23 September 1999, Santa Clara, California: Society of Photo-Optical Instrumentation Engineers, Electrochemical Society

### **Multilevel interconnections for ulsi and gsi era**

technology for the ULSI/GSI era of the silicon and (iii) minimum pitch local Also metals under consideration for multilevel interconnect application do

### **Ppt multilevel interconnect architectures**

Technology Power-aware interconnect design methodology strongly needed Task V Impact of inductance on multilevel ; interconnect n Tier Interconnect Network 22

### **Interconnect technology and design for gigascale**

Distributed RC and RLC Transient Models III J. Davis In recent years multi level interconnect networks have become the XII INTERCONNECT TECHNOLOGY AND

### **Patent us5612254 - methods of forming an**

A device and methods of forming an interconnection within a prepatterned channel in a semiconductor device are described. The present invention includes a method of

### **Ceramic interconnect technology handbook, iii,**

Ceramic Interconnect Technology Handbook - Kindle edition by III, the Ceramic Interconnect Technology Handbook is the only source for comprehensive discussion

### **Interconnect technology trend for**

with such astonishing advances the progress of interconnect technology still falls short 1.22: 30: 80: 1.05: 40: 83: 0 interconnect and multilevel

### **Electrochemical society [worldcat identities]**

Multilevel interconnect technology III : 22 and materials control in integrated circuit manufacturing V : 22-23 September, 1999, Santa Clara, Society of Photo

### **Divyesh desai - bokrecensioner**

"Multilevel Interconnect Technology III: 22-23 September 1999, Santa Clara, California", "Multilevel Interconnect Society for Optical Engineering, V. 3883.)

### **Mart graef - bokrecensioner**

Technology III: 22-23 September 1999, Santa 1999, Santa Clara, California (Proceedings of Spie--the International Society for Optical Engineering, V. 3883.)

### **Ild thermal stability in deep-submicron**

Multilevel interconnect technology III : ( Santa Clara CA, 22-23 September 1999 ) Multilevel Society of Photo-Optical Instrumentation Engineers,

### **Circuits and systems**

In Annual Meeting of the International Society for Magnetic Resonance in Medicine, In Proceedings of ISQED 2012, Santa Clara, CA, USA, September 1999.

### **Patent wo1999054521a2 - method and apparatus for**

manufactured by Applied Materials of Santa Clara, California, " MULTILEVEL INTERCONNECT TECHNOLOGY International Society for Optical Engineering,

### **Effects of nh {3} plasma treatment on methyl**

Plasma Treatment on Methyl Silsequioxane for Copper Multi-Level Interconnect the multi-level interconnect technology than the active (2.22 2.34) even if the

### **Electrochemical society - abebooks**

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### **International journal of application or innovation in**

in Proceedings of the 8th International Fuzzy Systems for aged power cables in IEEE Power Engineering Society, Santa Clara , CA) and Sherlock

### **Publications - fau**

Exhibition of the International Society for Sensor Networks (WiSNet), Santa Clara Photonics North Conference (SPIE Proceedings),

### **Patent ep0597087b1 - computer-aided design method**

Advanced Patent Search. Patents

### **Patent wo1993024896a1 - computer-aided design**

A computer-aided method of designing semiconductor interconnect structures for multilevel device an interactive SPICE subcircuit generator (22) and

### **Circuits and systems - tu delft**

In Annual Meeting of the International Society for Magnetic In Proceedings of the International Conference on Electromagnetics California, September

### **Spie | volume**

Santa Clara, CA | September 22, 1999 Processing your request Please Wait. Multilevel Interconnect Technology III, 160 (August 11, 1999);

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### **Brevetto us5739579 - method for forming**

A method for forming interconnections for semiconductor fabrication and semiconductor devices have such interconnections are described.

### **6640151 patent | multi-tool control system, method**

Multi-tool control system, method and medium (Los Altos Hills, CA), Grunes; Howard E. (Santa Cruz, CA) 23862973: Appl. No.: 09/469,227: Filed: December 22, 1999:

### **Patent us5610833 - computer-aided design methods**

display and computation tools for calculation and display of capacitance and other electrical characteristics of multilevel VLSI, PCB, and MCM interconnects.

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